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Form PTO-1449
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INFORMATION DISCLOSURE STATEMENT

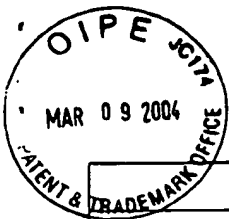
(Use several sheets if necessary)

APPLICANT
Yoshikazu KASUYAFILING DATE
October 22, 2003

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
✓.y.	1	6,255,166 B1	07/03/2001	Ogura et al.	7	1
↑	2	5,408,115	04/18/1995	Chang	11	1
	3	5,969,383	10/19/1999	Chang et al.	11	1
	4	5,422,504	06/06/1995	Chang et al.	11	1
	5	5,494,838	02/27/1996	Chang et al.	11	1
	6	6,177,318 B1	01/23/2001	Ogura et al.	11	1
	7	6,248,633 B1	06/19/2001	Ogura et al.	11	1
	8	US 2002-0100929	08/01/2002	Ebina et al.	11	1
	9	US 2002-0127805	09/12/2002	Ebina et al.	11	1
	10	6,413,821	07/02/2002	Ebina et al.	11	1
	11	6,518,124	02/11/2003	Ebina et al.	11	1
	12	US 2003-0054610	09/30/2003	Ebina et al.	11	1
	13	US 2003-0057505	03/27/2003	Ebina et al.	11	1
	14	US 2003-0058705	03/27/2003	Ebina et al.	11	1
	15	US 2003-0060011	03/27/2003	Ebina et al.	11	1
	16	US 2003-0190805	10/09/2003	Inoue	11	1
	17	US 2003-0186505	10/02/2003	Shibata	11	1
	18	US 2003-0166321	09/04/2003	Kasuya	11	1
	19 ⁱ	US 2003-0157767	08/21/2003	Kasuya	11	1
	20	US 2003-0166322	09/04/2003	Kasuya	11	1
	21	US 2003-0166320	09/04/2003	Kasuya	11	1
	22	US 2003-0211691	11/13/2003	Ueda	11	1
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Date: March 9, 2004



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	29	10/689,993	10/22/2003	Kasuya		
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
V4	30	JP A 2001-156188 (with abstract and translation)	06/08/2001	Japan	—	—
V4	31	JP A 7-161851 (with abstract and translation)	06/23/1995	Japan	—	—
V4	32	JP B1 2978477 (with abstract and translation)	09/10/1999	Japan	—	—
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)						
V4	33	Hayashi et al. "Twin MONOS Cell with Dual Control Gates", 2000 Symposium on VLSI Technology Digest of Technical Papers				
V4	34	Chang et al. "A New SONOS Memory Using Source-Side Injection for Programming", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp 253-255				
V4	35	Chen et al. "A Novel Flash Memory Device with S Plit Gate Source Side Injection and ONO Charge Storage Stack (SPIN), 1997 Symposium on VLSI Technology Digest of Technical Papers, pp 63-64				
EXAMINER				DATE CONSIDERED		
V. Gershon				05/04/04		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						

Date: March 9, 2004